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09/938,106	08/23/2001	James M. Derderian	4832US (01-0104)	1038

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	12

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/938,106	Applicant(s) DERDERIAN, JAMES M.	
	Examiner Junghwa M. Im	Art Unit 2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 29-69* is/are pending in the application.

4a) Of the above claim(s) *1-22, 36-39, 52 and 65-69* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-27, 29-35, 40-51 and 53-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent

Claims 23-24, 27, 29, 40, 45-46, 48, 49 and 59 are rejected under 35 U.S.C. 102(e) as being anticipated by Kondo et al. (US 6,545,365), hereafter Kondo.

Regarding claims 23 and 45, Fig. 4 of Kondo shows a device to use a method for assembling semiconductor devices with a densely stacked arrangement (col.1, lines 8-10), comprising; a first semiconductor device 3; discrete conductive elements 3a over portions of said first semiconductor device; positioning a second semiconductor device 6, 9 over the first semiconductor device and contacting at least some of said discrete conductive element with a back side of said semiconductor device with said back side and said at least some of discrete conductive elements electrically isolated from each other (col.2, lines 25-50 and col.3, line 1-14).

Regarding claims 24 and 46, Kondo discloses positioning the second semiconductor device comprises positioning the second semiconductor device on said at least some of discrete conductive elements with the back side and the discrete conductive elements in mutual electrical isolation (col.2, lines 25-50 and col.3, line 1-14).

Regarding claims 27 and 48, Kondo discloses positioning the second device a dielectric layer 9 in Fig. 4 at least portions of the back side.

Regarding claims 29 and 49, Kondo discloses a quantity of adhesive material 7 to at least an active surface of the first semiconductor device (col.2, lines 19-21).

Regarding claims 40 and 59, Kondo discloses securing the first semiconductor device and a substrate 2 to one another (col.2, lines 26-28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 23-27, 29-35, 40-51 and 53-64 are rejected under 35 U.S.C. 103(a) as being unpatentable under obviousness over Lee et al. (US 6,388,313), hereafter Lee in view of Foster (US 6,437,449) and Farnworth (US 5,012,323).

Regarding claims 23-24 and 45-46, Fig.1 of Lee shows a device to use a method for assembling semiconductor devices in stacked arrangement with the stacked arrangement having a height substantially equal to combined thicknesses of each of the semiconductor devices and distances discrete conductive elements associated therewith protrude above each semiconductor device, comprising:

providing a first semiconductor device 108 and 114 with discrete conductive elements 116, 122 and 124 protruding from an active surface of the first semiconductor device; and providing a second semiconductor device 140 and 146 at least partially over the first semiconductor device and at least some of the discrete conductive elements.

Lee shows a structure of a semiconductor substantially identical to the pending claim except the teaching of contact between the back of the second chip and discrete conductive elements and the mutual electrical isolation. Foster shows wires 122, 124 in Fig.1 are in contact with the back of the second chip, and Farnworth teaches an insulating layer covers an entire back side of the second chip (col.4, lines 47-54). It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Foster and Farnworth into the device of Lee to have electrical isolation of the two chips by providing an insulating layer on the back of the second chip to prevent a short circuit between two devices.

Regarding claims 25 and 47, Lee shows a method comprising: providing a dielectric coating on at least portions of the discrete conductive elements (col. 5, lines 40-44).

Regarding claim 26, Lee shows a method wherein the providing comprises forming at least one of a dielectric oxide and a dielectric polymer coating on at least said portions of the discrete conductive elements (col. 5, lines 22-24).

Regarding claim 27, Foster shows a forming a dielectric layer 146 in Fig. 2 at least portions of the back side.

Regarding claim 29, Lee shows applying a quantity of adhesive material to at least an active surface of the first semiconductor device (col. 5, lines 24-25).

Regarding claim 30, it is obvious that the device of Lee et al. show drawing the second semiconductor device toward the first semiconductor device after applying the adhesive on the first device.

Regarding claim 31, Lee shows the drawing is effected by at least one of capillary action of the adhesive material, curing of the adhesive material, application of

heat to the adhesive material, and vibration of the adhesive material (col. 5, lines 32-40).

Regarding claim 32, Foster shows applying an adhesive material 146 in Fig.4 on the back of the second device.

Limitations of claims 33-34 have been discussed above.

Regarding claim 35, Lee et al. show the drawing is effected during curing of the adhesive material (col. 5, lines 32-41).

Regarding claim 40, Lee shows securing the first semiconductor device and a substrate to one another (col. 5, lines 5-6).

Regarding claim 41, Lee shows wherein the placing the discrete conductive elements comprises securing the discrete conductive elements to contact areas of the substrate and the bond pads of the first semiconductor device (col. 5, lines 8-10).

Regarding claim 42, Lee shows the securing comprises electrically connecting bond pads of the second semiconductor device to the corresponding contacts areas of the substrate (col. 5, lines 13-16).

Regarding claim 43, Lee shows encapsulating at least portion of at least one of the substrate, the first semiconductor device, and the second semiconductor device (col. 6, lines 32-36).

Regarding claim 44, Lee shows forming external conductive elements 27 in Fig. 1 on the substrate in electrical communication with corresponding contact areas (col. 5, lines 1-4).

Limitations of claims 46-51 and 53-55 has been discussed above.

Regarding claim 56, Lee shows biasing at least one of the first and second

semiconductor devices toward the other of the first and second semiconductor devices (col. 4, lines 54-68).

Regarding claim 57, Lee shows controlling the biasing by means of adhesive (col. 4, lines 54-68).

Regarding claim 58, Lee shows the controlling the biasing comprises controlling the biasing force to a level sufficient to deform, kink, bend, or collapse the discrete conductive elements.

See the respective portions of the specification such as col. 5, lines 24-32.

Limitation of claim 59 has been discussed above.

Regarding claim 60, Lee shows connecting the discrete conductive elements to corresponding contact areas of the substrate (col. 5, lines 8-10).

Regarding claim 61, Lee shows establishing electrical communication between bond pads of the second semiconductor device and the corresponding contact areas of the substrate (col. 6, lines 8-12).

Regarding claim 62, Lee shows establishing communication comprises placing additional discrete conductive elements 25 in Fig. 1 between each of the bond pads and the corresponding contact area of the corresponding contact areas.

Limitations of claims 63 and 64 have been discussed above.

Claims 23 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable under over Foster in view of Farnworth.

Regarding Claims 23 and 45,as discussed above, Foster shows a structure of a

semiconductor substantially identical to the pending claim except the explicit teaching of electrical isolation between the back side of the second chip and the wires. Farnworth shows a packaging arrangement with the back of the second device is completely covered with an insulative film (col. 4, lines 49-52). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Farnworth to cover the entire back side of Foster's second device in order to have an electrical isolation from thr wires formed under the second chip preventing an short circuit.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi
May 18, 2003

Sara W Crane

Sara Crane
Primary Examiner